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(54) Configurable storage circuit

(57) A configurable storage circuit for a configurable logic element comprises memory means (121) for storing data and having at least a first and a second input lead. A first set of one or more input leads (F2, A) corresponding to the first input lead is provided to receive a corresponding input signal and a second set of one or more input leads (F1, D) corresponding to the second input lead is provided to receive a corresponding input signal. First means (123-125) has for each given lead of the first set, a corresponding configuration in which the first means provides the input signal on the given lead to the first input lead. Second means (128, 130, 132) has, for each given lead in the second set, a corresponding configuration in which the second means provides the input signal on said given lead to the second input lead. The memory means generates one or more output signals in response to the signals provided by the first and second means.

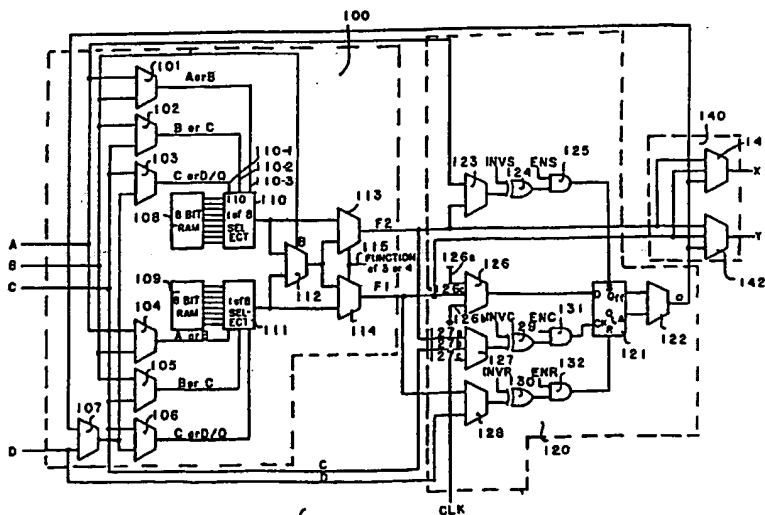


FIG. 8

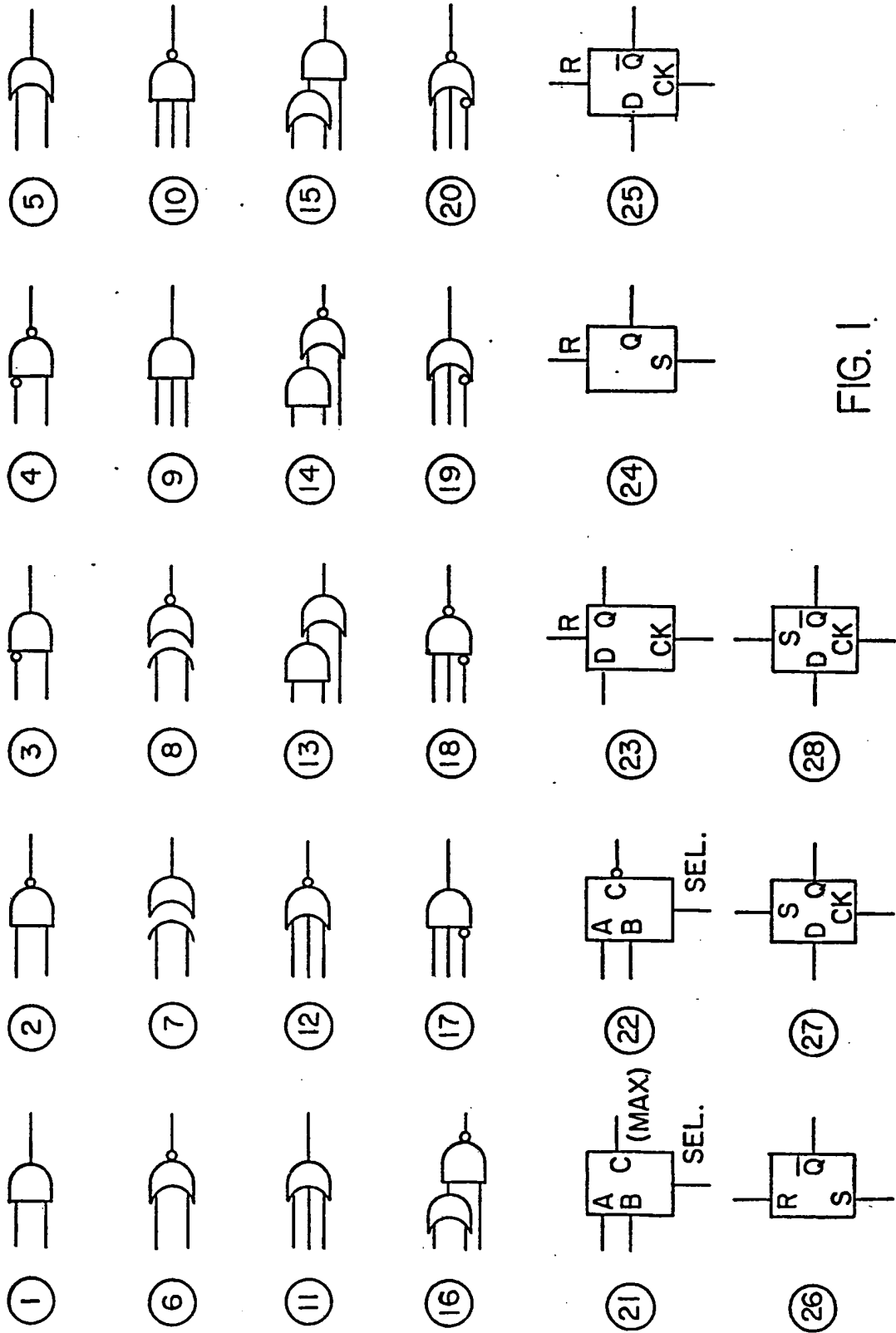
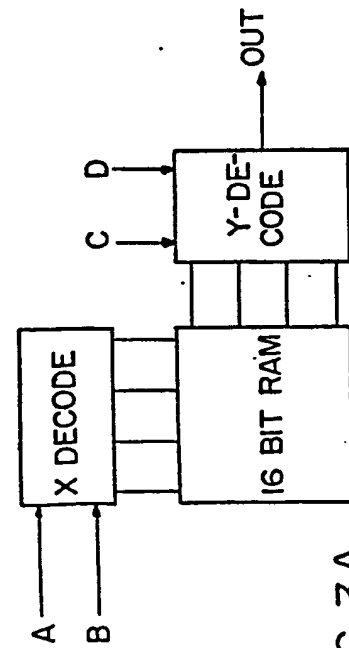
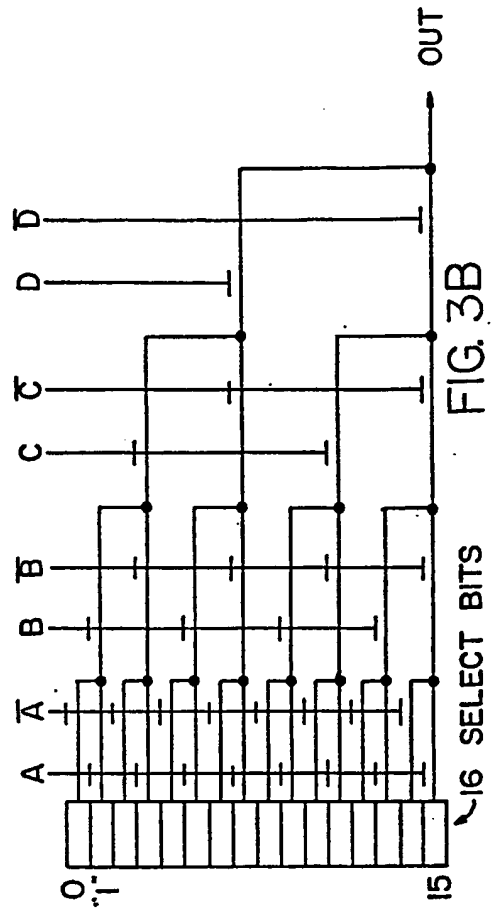
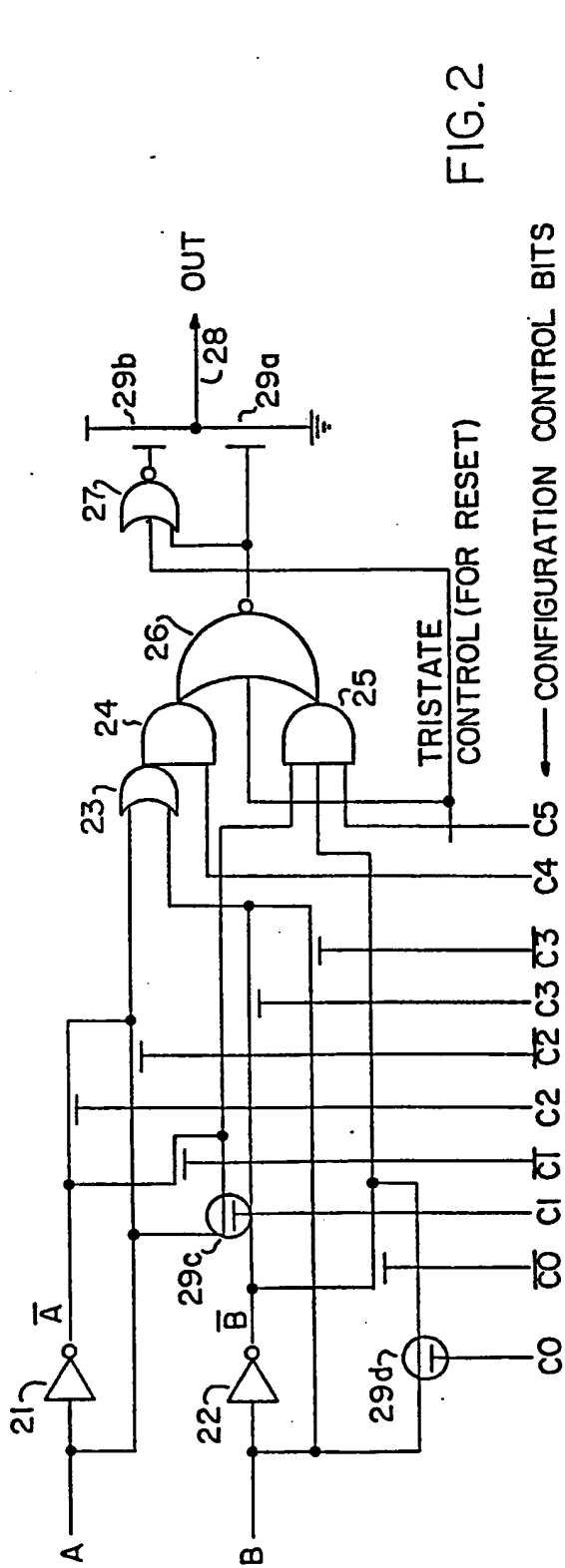


FIG. 1

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		C			
		0	1	1	0
A	D	0	0	1	1
	B				
0	0	1	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	1	0	0	0	0

FIG. 3C

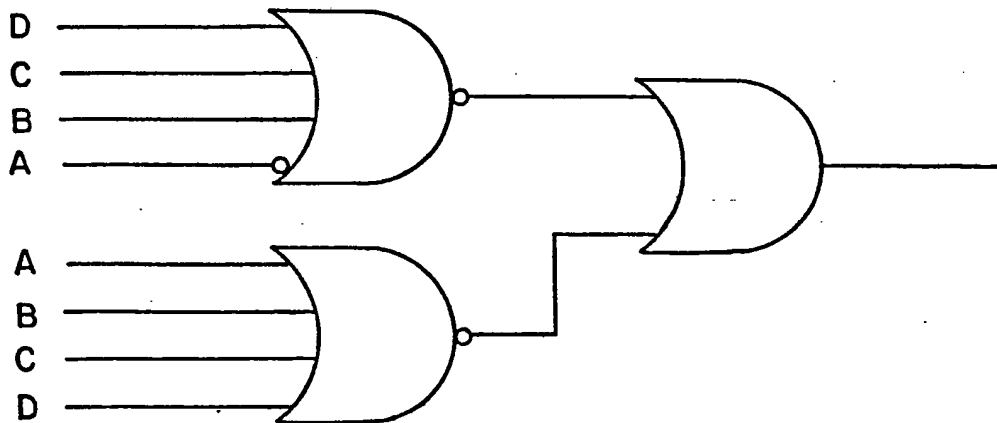


FIG. 3D

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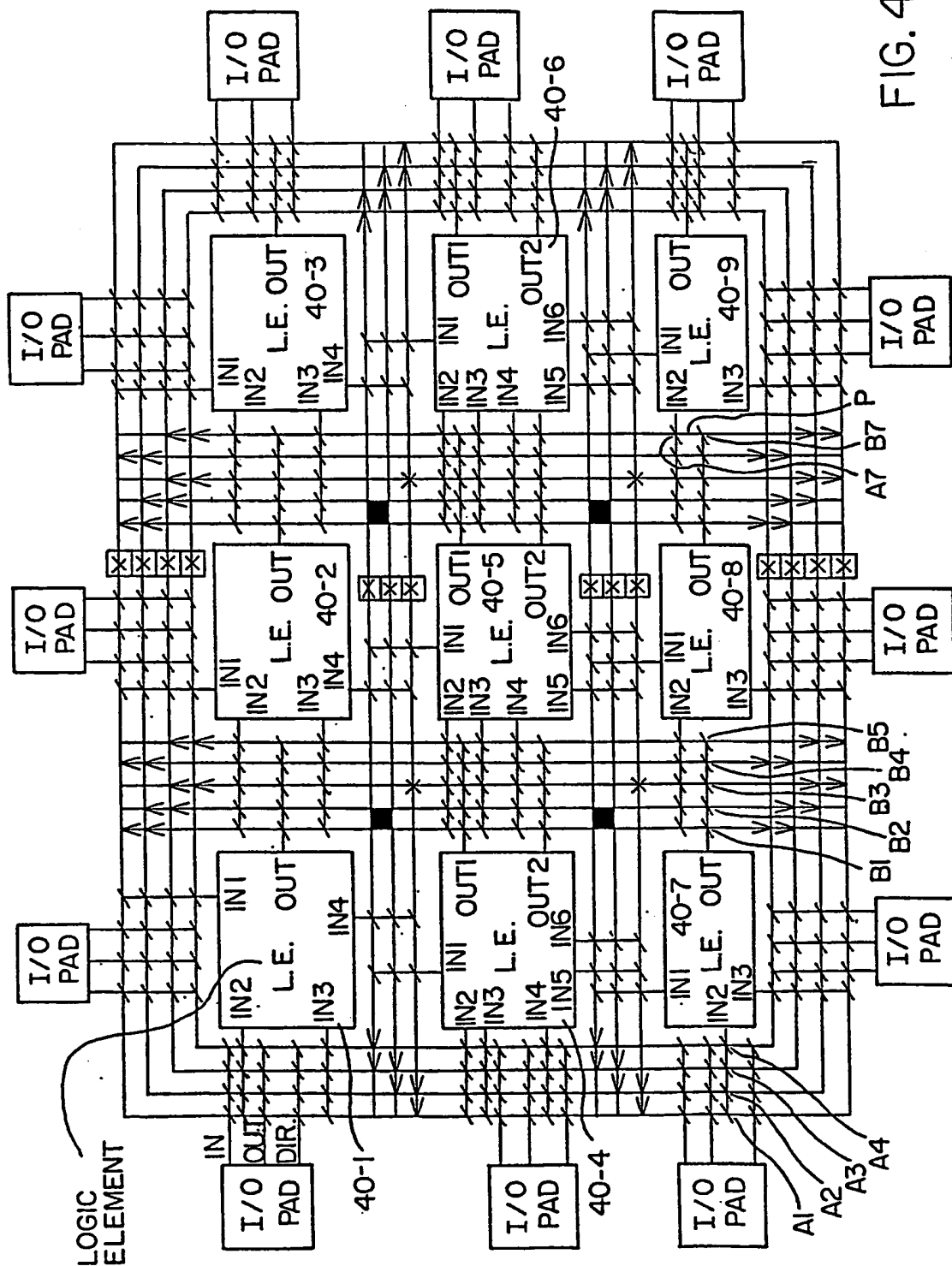


FIG. 4A

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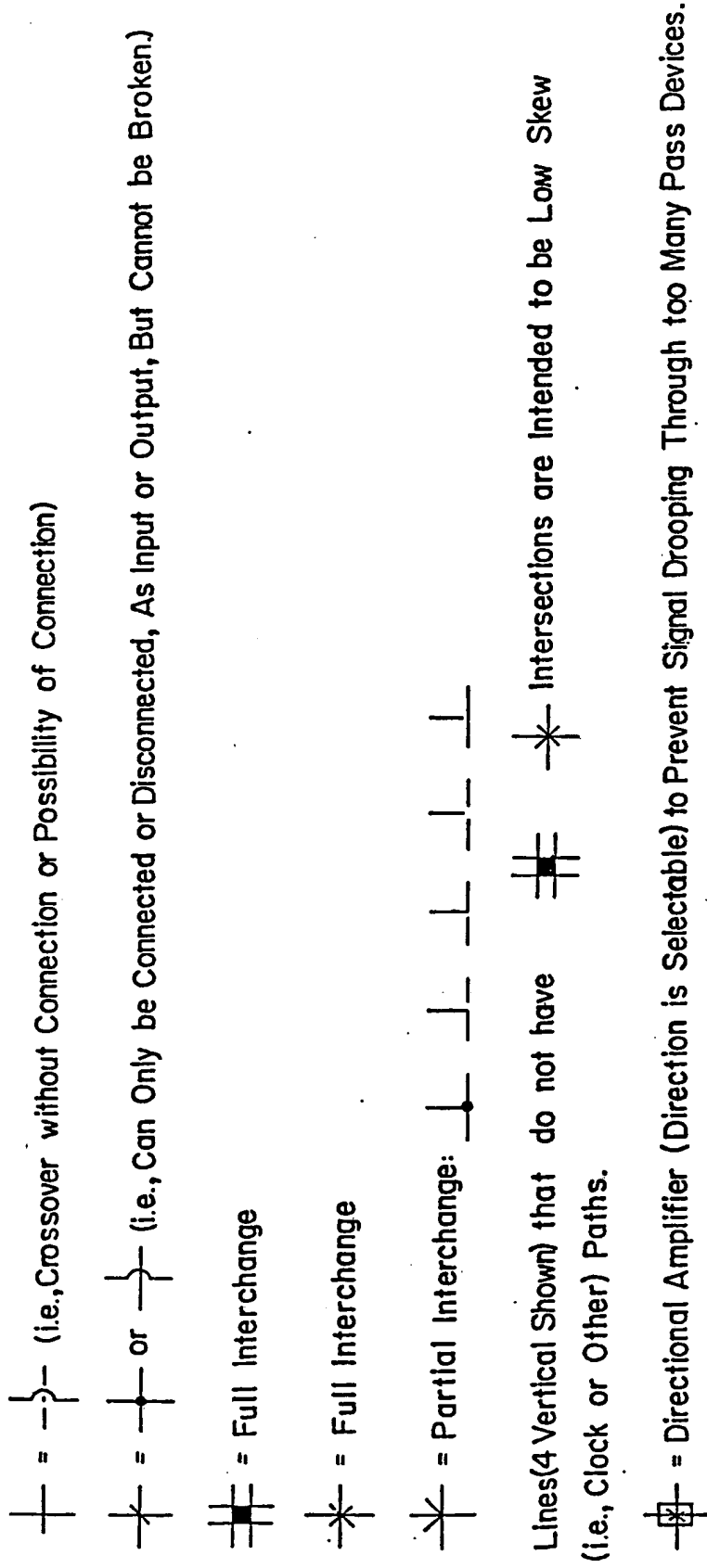


FIG 4B

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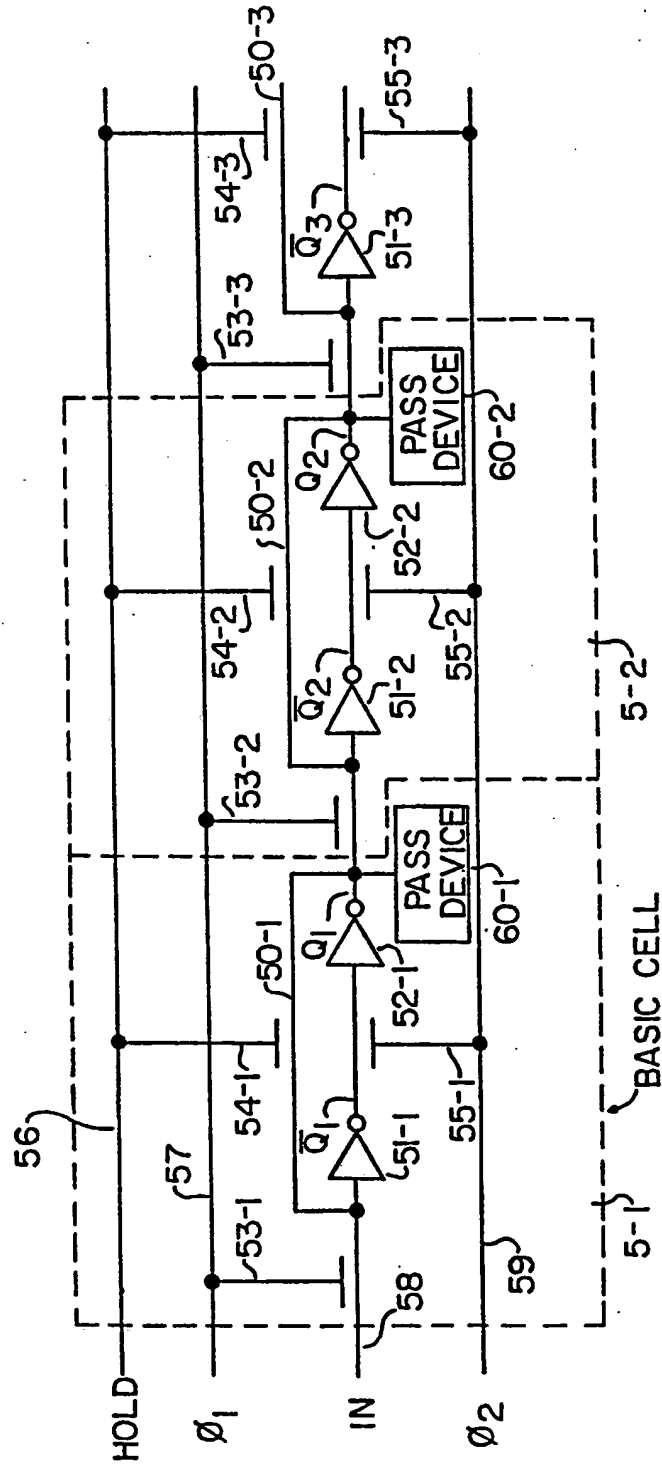
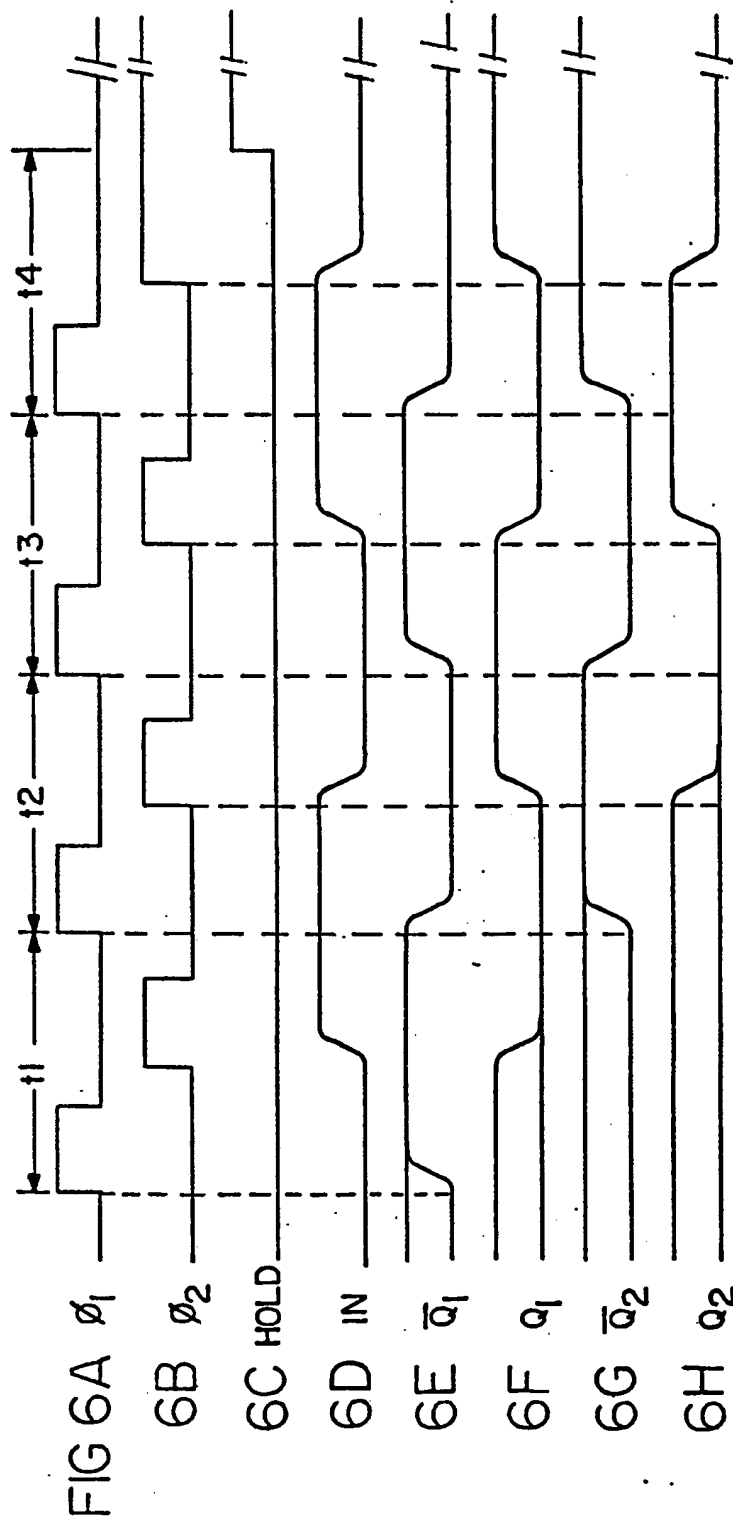


FIG. 5



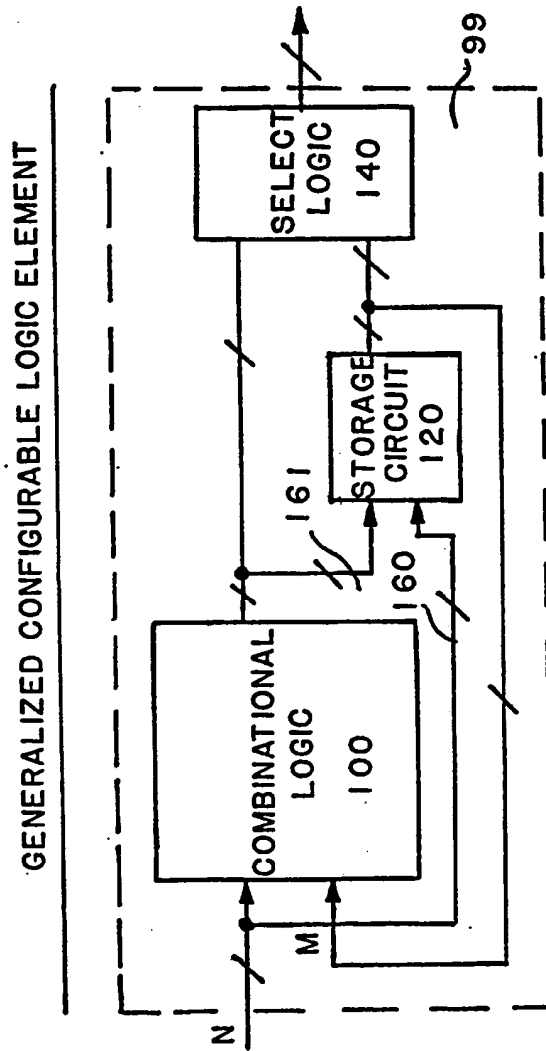


FIG. 7

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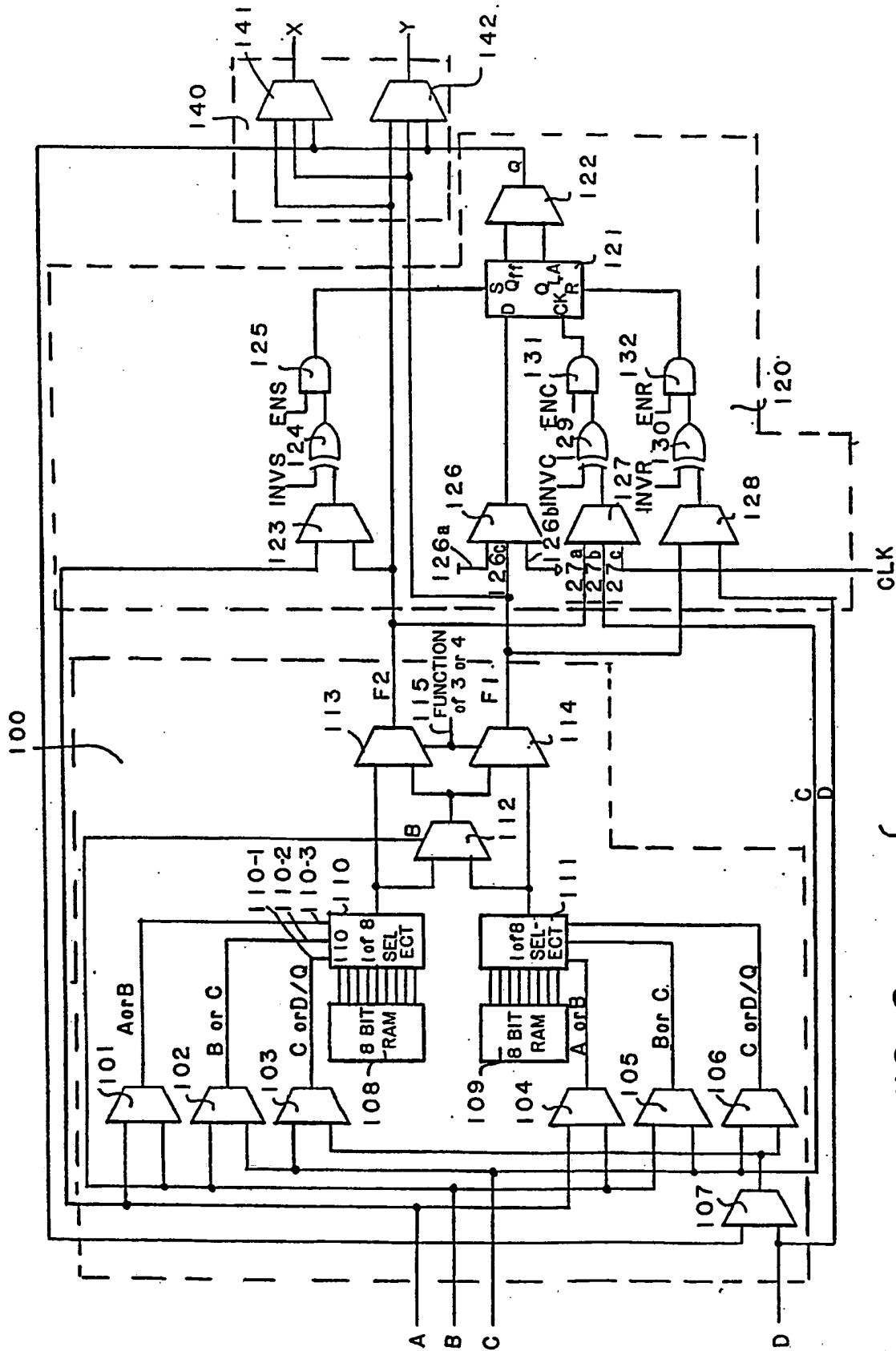


FIG. 8

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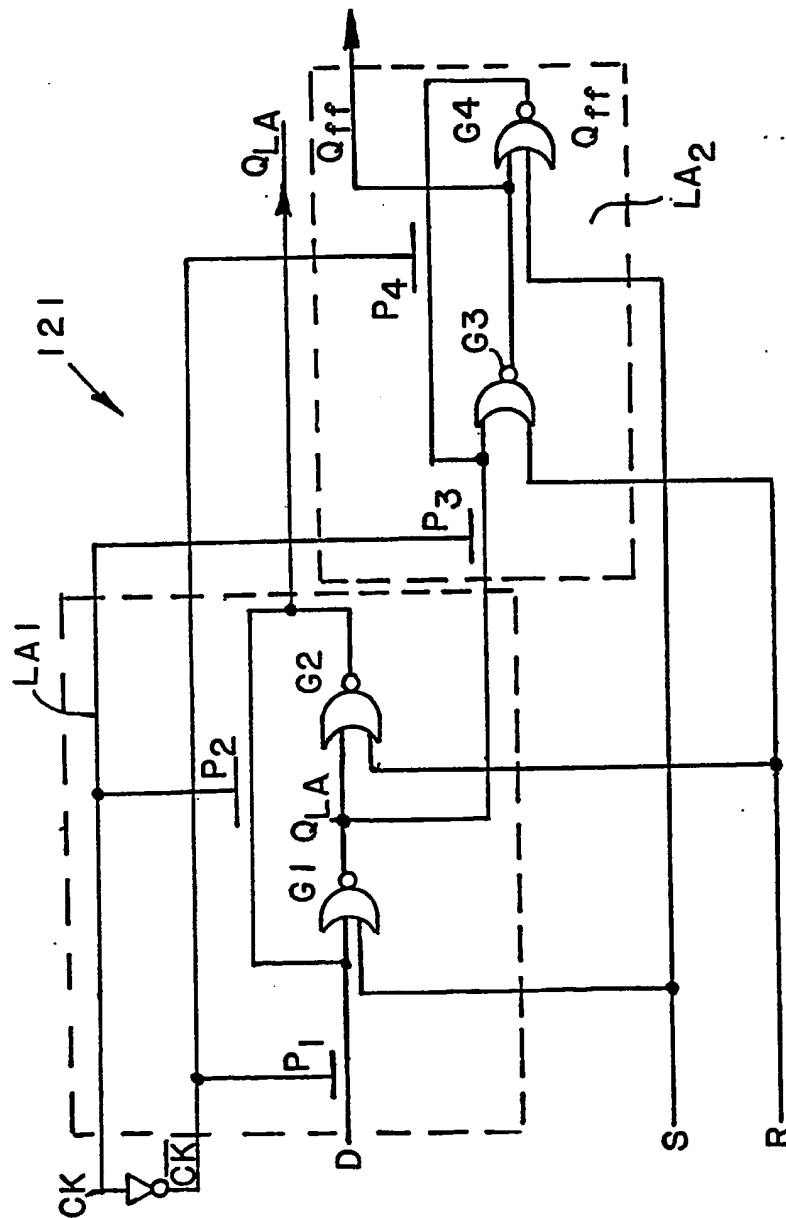


FIG. 9

R3810GB/ALM/mkf

Description of Invention

"Configurable storage circuit"

5 THIS INVENTION relates to configurable storage circuits and, in particular, to such a storage circuit for a configurable logic element which is composed of a configurable combinational logic circuit, the configurable storage circuit and a configurable output select logic. The output signals of the configurable storage circuit serve as input signals to both the configurable combinational logic circuit and the output select logic. The output signals of the output select logic are selected from the output signals of the combinational logic circuit and the output signals of the storage circuit.

15 In US Patent Application Serial No. 06/588,478, filed March 12, 1984 by Ross H. Freeman and entitled "CONFIGURABLE LOGIC ARRAY", a structure is described which allows changing the configuration of a finished integrated circuit from time to time (even when the integrated circuit is installed in a system) to provide any one of a plurality of logical functions from the same integrated circuit. This is accomplished by providing a number of "configurable logical elements" (herein referred to as "configurable logic elements") each of which is capable of being configured to implement any one of a plurality of logic functions depending on the task which it is called upon to perform. By configurable logic element is meant a combination of devices which are capable of being electrically interconnected by switches operated in response to control bits stored on the chip (or transmitted to the chip) to perform any one of a

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plurality of logical functions. The configurable logic element disclosed in Application No. 06/588,478 may include all of the circuit elements necessary to provide one or more of the functions provided by, for example, an AND gate, flip-flop, inverter, NOR gate, exclusive OR gate, and combinations of these functions to form more complex functions. The particular function to be carried out by a configurable logic element is determined by control signals applied to the configurable logic element from control logic. Depending on the control signals, a configurable logic element can function as an AND gate, an OR gate, a NOR gate, a NAND gate, or an exclusive OR gate or any one of a number of other logic functions without change in physical structure. Structure is provided on chip to allow any one of a plurality of functions to be implemented by the configurable logic element. This is done by providing control logic to store and generate control signals which control the configuration of the configurable logic element.

20 In one embodiment, the control signals are stored and transmitted by control logic formed integrally with and as part of the integrated circuit chip containing the configurable logic elements. However, if desired, the control information can be stored and/or generated outside the integrated circuit and transmitted through pins to the configurable logic element.

30 In general, a given set of control signals in the form of control bits is transmitted from the control logic to a configurable logic element to control the configuration of that configurable logic element. The actual set of control bits provided to the configurable logic element on the integrated circuit chip depends on the function to be carried out by the configurable logic element on the chip.

Our Co-pending Patent Application No. 8604761, from which the present Application is divided, claims a configurable logic element comprising: means for receiving a first plurality of N binary input signals; means for receiving a second plurality of M binary feedback signals; means for selecting K of said M+N binary signals (where $K \leq N+M$); combinational logic means for receiving said K binary signals from said means for selecting, said configurable combinational logic means having a plurality of configurations for generating binary output signals; a configurable storage circuit for receiving selected ones of said binary output signals of said configurable combinational logic means and selected ones of said N binary input signals and for generating said M binary feedback signals, said configurable storage circuit having a plurality of configurations; and a configurable select logic comprising means for receiving said output signals generated by said combinational logic means and said M binary signals generated by said configurable storage circuit and means for selecting output signals from among the signals received by said select logic.

The present invention provides a configurable storage circuit for such a configurable logic element, comprising: memory means for storing data, said memory means having at least a first and a second input lead; a first set of one or more input leads corresponding to said first input lead, each input lead of said first set for receiving a corresponding input signal; a second set of one or more input leads corresponding to said second input lead, each input lead of said second set for receiving a corresponding input signal; first means which, for each given lead in said first set, has a corresponding configuration in which said first means provides the input signal on said given lead to said first input lead; second means which, for each given lead

in said second set, has a corresponding first configuration in which said second means provides the input signal on said given lead to said second lead; said memory means generating one or more output signals in response to said signals provided by said first means and said second means.

In order that the invention may be more readily understood, an embodiment thereof will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 illustrates some of the various logic functions capable of being implemented by a configurable logic element in a configurable logic array;

Figure 2 illustrates the internal logic structure of one possible configurable logic element capable of implementing a number of useful functions of two variables A and B;

Figure 3A illustrates a 16 bit RAM circuit wherein any one of sixteen possible input states is capable of being identified and 2^{16} functions are capable of being implemented;

Figure 3B illustrates a selection structure for selecting any one of sixteen bits capable of implementing 2^{16} functions, for transmittal to an output lead;

Figure 3C illustrates one possible Karnaugh map for the structure of Figure 3A;

Figure 3D illustrates the logic gates represented by placing a binary one in the Karnaugh map of Figure 3C at the intersections of the first and second rows and the first column.

(
Figure 4A illustrates a plurality of configurable logic elements (shown as nine logic elements) formed on an integrated circuit chip together with programmable interconnects formed between selected leads to yield
5 desired logic functions and with selected input/output pads and interconnections of the leads between logic elements;

Figure 4B shows the key to the cross-connections
10 between crossing conductive leads in Figure 4A;

Figure 5 represents a portion of the circuitry of a novel combination static and dynamic shift register appropriate for use with the configurable logic array;

15 Figures 6A through 6H represent wave forms of use in explaining the operation of the structure of Figure 5;

Figure 7 shows a configurable logic element according to the invention of co-pending Application No. 8604761;
20

Figure 8 shows one embodiment of the configurable logic element of Figure 7 including a configurable storage circuit according to the present invention; and

25 Figure 9 shows one embodiment of a storage element included in the logic element of Figure 8.

The following detailed description of this invention is meant to be illustrative only and not
30 limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of the following disclosure.

Figure 1 illustrates certain logic functions capable of being implemented by a configurable logic
35 element. The _____

28 functions shown in Figure 1 are merely illustrative and other elements not shown can, if desired, be implemented by a configurable logic element. The following functions are shown:

<u>Element</u>	<u>Function</u>
1	AND gate
2	NAND gate
3	AND gate with inverted input
4	NAND gate with inverted input
5	OR gate
6	NOR gate
7	exclusive OR gate
8	exclusive NOR gate
9	3 input AND gate
10	3 input NAND gate
11	3 input OR gate
12	3 input NOR gate
13	OR gate with one input comprising AND gate
14	NOR gate with one input comprising AND gate
15	AND gate with one input comprising OR gate
16	NAND gate with one input comprising OR gate
17	3 input AND gate with one input inverted
18	3 input NAND gate with one inverted input
19	3 input OR gate with one inverted input
20	3 input NOR gate with one inverted input
21	one of two inputs multiplexer
22	inverting one of two inputs multiplexer
23	"D" flip flop with reset
24	Set-Reset latch
25	"D" flip-flop with reset and inverted output
26	Set-reset latch with reset and inverted output.
27	"D" flip-flop with set
28	"D" flip-flop with set and inverted output

Of course, other logic functions can also be implemented in a configurable logic element.

Figure 2 illustrates the internal logic structure of one possible configurable logic element which is capable of implementing all useful basic functions of the two variables A and B, with the functions being selected by configuration control signals C_0 , \bar{C}_0 , C_1 , \bar{C}_1 , ... through C_5 on control leads C_0 , \bar{C}_0 , ... through C_5 . (In this example, all control leads are connected to the gates of N channel enhancement mode pass transistors.) To implement an AND gate function using the structure shown in Figure 2, the input leads labeled A and B are shunted past inverters 21 and 22, respectively, to AND gate 25 by high level signals on the C_1 and C_0 configuration control leads which, being connected to the gates of N channel enhancement mode pass transistors 29c and 29d, cause pass transistors 29c and 29d to turn on.

Low level signals are applied to the configuration control leads \bar{C}_0 and \bar{C}_1 , thus blocking the output signals of inverters 21 and 22 from AND gate 25. In addition, a high level signal on lead C_5 is applied to enable AND gate 25. Thus three input AND gate 25 functions as a two-input AND gate with respect to the signals A and B. The output signal of AND gate 25 provides one input signal to NOR gate 26. A second input signal to NOR gate 26 is provided by the output signal of AND gate 24. The output signal of AND gate 24 is held at a logical 0 by applying a logical 0 to configuration control lead C_4 . Thus the control signals C_2 and C_3 are "don't cares", that is, these signals can be high or low without affecting the output signal of AND gate 24. Since the output signal of AND gate 24 is a logical 0, and since the tri-state control input signal to NOR gate 26 is a logical 0, it is easy to see that AND gate 25, AND gate 24 and NOR gate 26 function together as a NAND gate with respect to input signals A and B. Since the tri-state control signal input to NOR gate 27 is a logical 0 (except during reset), NOR gate 27 serves as an inverter with respect to the output signal of NOR gate 26. The output

1 signal of NOR gate 26 is applied to the gate of N channel
2 transistor 29a (the source of which is grounded and the
3 drain of which is connected to output lead 28) and the
4 complement of the output signal of NOR gate 26 is applied
5 to the gate of N channel transistor 29b (the source of
6 which is connected to a power supply and the drain of
7 which is connected to both the output lead 28 and the
8 drain of N channel transistor 29a). Thus, transistors
9 29a and 29b function as an inverter with respect to the
10 output signal of NOR gate 26. Thus, the structure of
11 Figure 2 configured as described above performs the
12 function of an AND gate with respect to the signals A and
13 B. Other logic functions can also be produced by appro-
14 priate selection of the control signals to be supplied to
15 the configuration control leads C0 through C5 to activate
16 the appropriate pass transistors and gates within the
17 structure.

18 Figure 3A illustrates a 16 bit RAM capable of producing
19 an output signal in response to any one of sixteen possible
20 combinations of input signals. Thus input signals A and
21 B control the X decoder to select any one of the four
22 columns in the 16 bit RAM. Input signals C and D control
23 the Y decoder to select any one of the four rows in the
24 16 bit RAM. The 16 bit RAM produces an output signal
25 representative of the bit at the intersection of the
26 selected row and column. There are 16 such intersections
27 and thus sixteen such bits. There are 2^{16} possible
28 combinations of functions capable of being represented by
29 16 bits. Thus, if a NOR gate is to be simulated by the
30 16 bits in the RAM, the Karnough map for the RAM would be
31 as shown in Figure 3C. In Figure 3C all bits are "0"
32 except the bit at the intersection of the first row
33 (representing A=0, B=0) and the first column (representing
34 C=0, D=0). Should a less frequently used function be
35 desired to be generated by the 16 bit RAM, (for example,
36 should a "1" output signal be desired for A=1, B=0, C=0
37 and D=0) then a binary "1" is stored at the intersection
38

1 of the second row and the first column. Should a binary
 2 "1" be desired both when $A=0$, $B=0$, $C=0$ and $D=0$ and also
 3 when $A=1$, $B=0$, $C=0$ and $D=0$, then a binary "1" is stored
 4 at each of the intersections of the first column with the
 5 first row and the second row. The logic circuit repre-
 6 sented by this loading of the RAM is as shown in Figure
 7 3D. Thus the RAM of Figure 3A represents an elegant and
 8 simple implementation of any one of 2^{16} logic functions.

9 Figure 3B shows another structure for yielding any
 10 one of sixteen select bits. Each of registers 0-15 in
 11 the vertical column to the left labeled "16 Select Bits",
 12 contains a selected signal, either a binary 1 or 0. By
 13 selecting the proper combination of A, B, C, and D, a
 14 particular bit stored in a particular one of the sixteen
 15 locations in the 16 Select Bits register is transmitted
 16 to the output lead. Thus, for example, to transmit the
 17 bit in the "1" register to the output lead, the signal A,
 18 B, C, D is applied to the leads so labeled. To transmit
 19 the signal labeled "15" in the sixteenth location in the
 20 16 Select Bits register to the output lead, the signal A,
 21 \bar{B} , \bar{C} , and \bar{D} is applied to the appropriate columns.
 22 Again, any one of 2^{16} logic functions can be implemented
 23 using this structure.

24 Figures 4A illustrates a configurable logic array
 25 containing nine configurable logical elements. As shown
 26 in Figure 4a, each CLE of the nine CLEs 40-1 through 40-9
 27 has a plurality of input leads and one or more output
 28 leads. Each input lead has a plurality of access junctions
 29 each connecting a selected general interconnect lead to
 30 the input lead. The access junctions for input lead 2 of
 31 CLE 40-7 are labeled A1 through A4 in Figure 4a. The
 32 access junctions for the other input leads are indicated
 33 schematically but are not labeled for the sake of clarity.
 34 Similarly, each output lead of each CLE has a plurality
 35 of access junctions each connecting the output lead to a
 36 corresponding one of the general interconnect leads. The
 37 access junctions are indicated schematically for each
 38

1 output lead of each CLE in Figure 4a. The access junc-
2 tions for the output lead of CLE 40-7 are labeled B1
3 through B5. The leads in Figure 4a which are neither
4 input leads nor output leads are called general inter-
5 connect leads and the junctions in Figure 4a which are
6 not access junctions for input and output leads are
7 called general interconnect junctions. As shown in
8 Figure 4A, nine logic elements are placed on an integrated
9 circuit chip together with programmable access junctions
10 and a general interconnect structure which comprises
11 general interconnect leads and programmable general
12 interconnect junctions for connecting various leads to
13 other leads. The general interconnect structure includes
14 a set of general interconnect leads and of programmable
15 junctions interconnecting the general interconnect leads
16 having the property that for each general interconnect
17 lead in the general interconnect structure there is a
18 programming of the general interconnect junctions which
19 connects the given general interconnect lead to one or
20 more other leads in the general interconnect structure.
21 Moreover, there is a programming of the junctions (both
22 access and general interconnect) such that for any given
23 output lead of any CLE in the CLA, and for any given
24 input lead of any other CLE in the CLA, there is a pro-
25 gramming of the junctions such that the given output lead
26 is connected to the given input lead. An electrical path
27 from a given output lead to a given input lead always
28 contains at least two access junctions and at least a
29 portion of a general interconnect lead. For example, one
30 electrical path from the output lead of CLE 40-8 to the
31 second input lead of CLE 40-9 contains access junctions
32 A7 and B7 and the marked portion P of a general intercon-
33 nect lead. Typically, an electrical path from an output
34 lead of one CLE to an input lead of another CLE will also
35 contain one or more general interconnect junctions. Each
36 of logic elements 40-1 through 40-9 represents a collection
37 of circuitry such as that shown in Figure 2 or some
38

1 similar structure capable of being configured as described
2 above in Figure 2 to perform any one of a number of logic
3 functions. To program the circuitry (both the configurable
4 interconnect switches and the configurable logic elements),
5 selected signals are applied to input leads identified as
6 configuration control input leads thereby to generate a
7 desired logical function in each of the logic elements
8 and to interconnect the logic elements as desired. In
9 Figure 4A, no specific lead has been identified as an
10 input lead for the configuration control signals. However,
11 any particular I/O pad can be selected for this purpose.
12 The configuration control bits can be input into the
13 configurable logic array either in series or in parallel
14 depending upon design considerations where they are
15 typically stored in a programming register (shown in
16 Figure 5). Alternatively, the configuration control bits
17 may be stored in a memory on chip. In addition, another
18 I/O pad will be used for an input clock signal which is
19 used, inter alia, for the loading of the configuration
20 control signals into the programming register. When the
21 configurable logic array shown in Figure 4A has been
22 configured, selected output signals of logic elements
23 40-1 through 40-9 are provided to selected I/O pads.
24 Figure 4B illustrates the meaning of the junction symbols
25 used in Figure 4A.

26 To configure a logic element such as logic element
27 40-1 (Figure 4A), a number of bits must be applied to the
28 configuration control leads such as leads C0 through C5,
29 as shown, for example, in Figure 2. To do this a shift
30 register, for example, is utilized as part of each configu-
31 rable logic element. Figure 5 illustrates a shift register
32 which may be used. The shift register of Figure 5 is
33 illustrated showing two basic storage cells. Each storage
34 cell is capable of storing one bit of information. Of
35 course, an actual shift register will contain as many
36 storage cells as required to configure the logic element
37 of which the shift register is a part, to its desired
38

1 configuration. In operation, an input signal is applied
 2 to input lead 58. This input signal (shown in Figure 6D)
 3 contains bit stream to be stored in the shift register as
 4 configuration control bits to configure the configurable
 5 logic element to perform a desired logic function or to
 6 configure (program) an access junction or a general
 7 interconnect junction between general interconnect leads
 8 in a manner to be described shortly. Thus the sequence
 9 of pulses applied to input lead 58 represents those
 10 pulses which when stored in the storage cells of the
 11 shift register will activate the configuration control
 12 bits in the proper manner to achieve the desired functional
 13 and/or interconnection result. For example, if the
 14 circuit of Figure 2 is to be configured to form an AND
 15 gate, the pulses C0, C1, C2, C3, C4, and C5 would be
 16 represented by 1,1,X,X, 0,1.

17 The sequence of pulses applied to input lead 58 is
 18 synchronized with clocking pulses $\phi 1$ and $\phi 2$ applied to
 19 leads 57 and 59 respectively. Thus in the first period
 20 of operation clocking pulse $\phi 1$ goes high (Fig. 6A),
 21 clocking pulse $\phi 2$ is low (Fig. 6B), the hold signal (Fig.
 22 6C) is low during shifting thereby facilitating the
 23 passage of data through sequentially connected cells 5-1,
 24 5-2 et al. of the shift register. To shift the pattern
 25 01010 into the shift register, the following operations
 26 occur: The input signal on lead 58 is low during approx-
 27 imately the first half cycle of the clocking period t_1 .
 28 The output signal $\bar{Q}1$ of inverter 51-1 goes to a high
 29 level in response to the low level input signal and $\phi 1$
 30 high to enable pass transistor 53-1. Some time through
 31 the first clocking period t_1 , the clock signal $\phi 1$ goes
 32 low (Fig. 6A) and the clock signal $\phi 2$ shortly thereafter
 33 goes high (Fig. 6B) to enable pass transistor 55-1.
 34 Consequently, the high level output signal $\bar{Q}1$ is trans-
 35 mitted to the input lead of inverter 52-1 by enabled pass
 36 transistor 55-1 and thereby produces a low level output
 37 signal Q1 on the output lead of inverter 52-1. Thus at
 38

1 the end of period t_1 , the output signal Q_1 (Figure 6F)
 2 from inverter 52-1 is low level. The output signals \bar{Q}_2
 3 and Q_2 from inverters 51-2 and 52-2 in the second cell
 4 are still indeterminate because no known signal has yet
 5 propagated to the second storage cell 5-2 to change the
 6 signals of these inverters to a known state.

7 At the beginning of the second period (labeled " t_2 "
 8 in Fig. 6A), ϕ_1 goes high (Fig. 6A) and ϕ_2 is low (Fig.
 9 6B) having gone low before period t_1 ended. The input
 10 signal (Figure 6D) now has risen to a high level repre-
 11 senting a binary 1 and thus the output signal \bar{Q}_1 of
 12 inverter 51-1 has gone low. The output signal Q_1 of
 13 inverter 52-1 remains low because pass transistor 55-1 is
 14 held off by the low level ϕ_2 signal. Some time through
 15 the second period ϕ_1 goes low followed a fraction of time
 16 later by ϕ_2 going high. At this time, the output sig-
 17 nal \bar{Q}_1 is transmitted through pass transistor 55-1 to
 18 inverter 52-1 thereby driving the output signal Q_1 from
 19 inverter 52-1 to high level. Meanwhile, during period t_2
 20 the previous low level signal on Q_1 has driven the output
 21 signal \bar{Q}_2 of inverter 51-2 to a high level when Q_1 was at
 22 a high level to enable pass transistor 53-2 and the
 23 change in ϕ_2 from a low level to a high level in the
 24 second half of period t_2 to enable pass transistor 55-2
 25 drives the output signal Q_2 from inverter 52-2 to a low
 26 level. In this manner, the input signal on lead 58 (Fig.
 27 6D) is transmitted through each of the cells 5-1, 5-2,
 28 5-3 et al. in the shift register. Upon the transfer into
 29 the shift register of the desired information, the hold
 30 signal (Figure 6C) is enabled (i.e., driven to a high
 31 level) thereby to connect the feedback leads 50-1, 50-2,
 32 and 50-3 et al. from the output leads of inverters 52 to
 33 the input leads of inverters 51 so as to hold the infor-
 34 mation then in each cell indefinitely. In operation, the
 35 signal stored in a given cell e.g. 5-1 is connected to a
 36 configuration control or to an interconnect pass device,
 37 such as devices 60-1 and 60-2 illustrated schematically
 38 in Figure 5.

The output signals Q_1 , \bar{Q}_1 , Q_2 , \bar{Q}_2 , etc., of the shift register are directly connected to the (configuration) control inputs of a logic element or the pass devices of the general interconnect junctions.

5

When ϕ_1 is low, ϕ_2 and hold may be brought high, thus holding the data indefinitely. The entire shift register may be set or cleared by setting or clearing the input with ϕ_1 and ϕ_2 both high and HOLD low. Enough set/reset time must be allowed for the signal to propagate the entire length of the shift register to clear the shift register in this manner. Naturally this time is dependent upon the length of the shift register.

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The shift register operates in its dynamic phase by storing the information being shifted as charge on the gates of the transistors (not shown in Figure 5 but well known) comprising inverters 51-1, 52-1, 51-2, 52-2 et al of the shift register. These inverters are of well-known design and will not be described in detail. The use of a dynamic shift register is important because a dynamic shift register uses six transistors and thus takes up very little area. The dynamic shift register is converted to a static latch by adding only one transistor. Thus the dynamic shift register (static latch) can be easily fabricated as part of a configurable logic element without adding significant complexity to the circuit or consuming significant semiconductor area. Because of the "hold" signal, the dynamic shift register can become a static latch because placing the shift register on hold automatically refreshes the data. Thus a separate refresh circuit is not needed.

25

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It is apparent from the above description that the dynamic shift register (static latch) circuit does not need refreshing once it has been latched into a hold state. This is accomplished by use of the feedback circuit comprising lead 50-1 and pass transistor 54-1 in cell 5-1, for example.

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1 Fig. 7 shows a block diagram of the configurable
 2 logic element 99 of the present invention which includes
 3 configurable combinational logic 100, configurable stor-
 4 age circuit 120 and configurable output select logic 140.
 5 The combinational logic 100 receives the N binary input
 6 signals to the configurable logic element 99 and M binary
 7 "feedback" signals from storage circuit 120. Combinational
 8 logic 100 is configurable into a plurality of configura-
 9 tions. Each configuration implements one or more selected
 10 combinational logic functions of one or more selected
 11 subsets of the input signals to the combinational logic.
 12 Since combinational logic 100 is configurable, it can be
 13 employed to implement a variety of different functions.
 14 Moreover, two or more selected functions may be implemented
 15 simultaneously, appearing on separate output leads of the
 16 configurable logic element 100. In more detail, combina-
 17 tional logic 100 selects K binary input signals from
 18 among its M+N binary input signals ($K \leq M+N$). Combinational
 19 logic circuit 100 is responsive to a plurality of sets of
 20 values of a first set of configuration signals including
 21 at least a first set of values for which configurable
 22 combinational logic 100 implements a first set of func-
 23 tions, each of which is a function of some of said K
 24 binary signals, and a second set of values for which
 25 configurable combinational logic 100 implements a second
 26 set of functions, each of which is a function of some of
 27 said K binary signals, where said first set of functions
 28 is not the same as said second set of functions. In one
 29 embodiment combinational logic 100 has a first configura-
 30 tion which implements a selectable 1 of the 2^{2^K} binary
 31 valued functions of these K binary signals and a second
 32 configuration which implements both a selectable 1 of the
 33 $2^{2^{(K-1)}}$ binary valued functions of a first selected (K-1) of
 34 the K selected binary input signals and a selectable 1 of
 35 the $2^{2^{(K-1)}}$ binary value functions of a second selected (K-1)
 36 of the K selected binary input signals. . (The second set

1 of K-1 signals need not be distinct from the first set.)
2 The operation of combinational logic 100 will be more
3 readily understood after a consideration of the specific
4 embodiment described in Fig. 8 which is explained hereafter.

5 Storage circuit 120 is also configurable and may be
6 programmed to implement, depending on the configuration,
7 one or more storage elements each of which may be, for
8 example, a transparent latch with set and reset, a D
9 flip-flop with set and reset, an edge detector, a stage
10 of a shift register, or a stage of a counter. Configurable
11 storage circuit 120 receives the output signals of combina-
12 tional logic 100 on bus 161 as well as a clock signal and
13 selected ones of the N input signals of combinational
14 logic 100 on input bus 160. Output select logic 140 is
15 configured to provide output signals which are selected
16 from among the output signals of the combinational logic
17 element and the storage circuit.

18 Fig. 8 shows the details of one embodiment of the
19 configurable logic element 99 in Fig. 7. In Fig. 8, the
20 four input signals to the configurable logic element 99
21 are denoted by A, B, C, D (i.e., N=4). Since the storage
22 circuit 120 provides only a single feedback signal Q to
23 switch 107, M=1. In Fig. 8, K=4 since the signals A, B,
24 C and either D or Q are selected from among the five
25 signals A, B, C, D, and Q. Configurable combinational
26 logic element 100 includes configurable switches 101
27 through 107, 113, and 114, 8-bit RAMs 108 and 109, one of
28 eight select logics 110 and 111, multiplexer 112, and
29 configuration control lead 115 to switches 113 and 114.
30 Each of the configurable switches is configured by control
31 bits from a programming register (not shown) on leads
32 (not shown except for lead 115) as previously explained.
33 Switch 101 may be configured to provide signal A as its
34 output signal or it may be configured to provide signal B
35 as its output signal. Similarly, each of the switches
36 102 through 107 may be configured to provide a selected 1
37 of its two input signals as its output signal. Thus, for
38 example, for one selection of configuration control bits,

1 switch 107 provides signal D and the binary signals A, C,
 2 and D are provided to both one of eight select logic 110
 3 and one of eight select logic 111 by switches 101 through
 4 103 and 104 through 107, respectively. For each of the
 5 eight possible combinations of binary signals A, C and D,
 6 select logic 110 selects a unique storage element in RAM
 7 108 and outputs the bit stored in the selected location.
 8 One of eight select logic 111 operates similarly with
 9 respect to 8-bit RAM 109. Multiplexer 112 provides
 10 either the output signal from select logic 110 or the
 11 output signal from select logic 111, depending on the
 12 state of signal B. For this configuration, the control
 13 bit applied on lead 115 causes switches 113 and 114 to
 14 simultaneously pass the output signal from multiplexer
 15 112 to output leads F1 and F2 of combinational logic
 16 element 100. The two 8-bit RAMs 108 and 109 can be
 17 programmed with binary bits in 2^{16} different ways. Each
 18 choice of programming of the 8-bit RAMs causes the combi-
 19 national logic of element 100 to implement one of the
 20 $2^{16}=2^{2^4}$ possible logic functions of the four binary
 21 variables A, B, C and D. (Here $K=4$.) (A logic function
 22 is a binary valued function of binary variables.)
 23

24 For another selection of configuration control bits,
 25 switch 107 provides feedback signal Q from storage circuit
 26 120 and switches 101 through 103 and 104 through 107 and
 27 113 and 114 are configured as before. Then the combina-
 28 tional logic element 100 implements one of the $2^{16}=2^{2^4}$
 29 possible logic functions of the four binary variables A,
 30 B, C and Q for each choice of programming of the two 8
 31 bit rams 108 and 109. (Here again $K=4$.)
 32

33 For another selection of configuration control bits,
 34 switches 101 through 103 provide signals A, C and Q, and
 35 switches 104 through 106 provide signals B, C, and Q,
 36 respectively, and the control signal applied to lead 115
 37 causes switches 113 and 114 to provide the output signal
 38 of select 110 on lead F2 and the output signal of se-
 lect 111 on lead F1, respectively. Thus, this configura-

tion implements on lead F1 one of the $2^8=2^{2^3}$ logic functions of the three binary variables A, C, and Q for each of the 2^8 possible programmings of 8-bit RAM 108 and on lead F2 implements one of the 2^8 logic functions of the three binary variables B, C and Q for each of the $2^8=2^{2^3}$ possible programmings of RAM 109.

In general, for any first selection of three of the four variables A, B, C and D/Q, and for any second selection of three of the four variables A, B, C and D/Q, there is a configuration of the combinational logic element 100 which implements one of the 2^{2^3} logic functions of the first selection of three variables on output lead F2 for each of the 2^8 possible programmings of 8-bit RAM 108 and one of the 2^{2^3} logic functions of the second selection of three variables on output lead F1 for each of the 2^8 possible programmings of RAM 109.

In another embodiment (not shown), each of the 8-bit RAMs may be "subdivided" by providing each with two additional one of four select logic so that any four binary functions of two of the variables A, B, C and D/Q are implemented on four additional output leads of the combinational logic element 100. Similarly, in another embodiment (not shown) a 32 bit RAM and the signals A, B, C, and D and the feedback signal Q are all used (so that $K=5$) to implement in one configuration one of the 2^{2^5} binary functions corresponding to each programming of the 32 bit RAM (here $N=4$, $M=1$, and $K=5$) In another configuration (not shown) $N=4$, $M=1$, $K=5$, and a first binary function F1 of the variables A, B, C a second binary function F2 of the variables B, C, D and a third binary function F3 of the variables B, C, D, Q are implemented. It is important to observe that $2^{K'_1} + 2^{K'_2} + 2^{K'_3} = 2^K$ where K'_i is the number of variables of which F_i is a function for $i=1, 2, 3$. Returning to Figure 8, it is also important

1 to observe that configurable switches 101, 102 and 103
2 select a subset of their input signals and provide the
3 selected subset of input signals on a one-to-one basis to
4 selected input leads of circuit 110. For example, in
5 response to one set of values of configuration signals,
6 configurable switches 101, 102 and 103 provide signal A
7 to lead 110-3, signal B to lead 110-2, and signal C to
8 lead 110-1.

9 The output signals on leads F1 and F2 are input
10 signals to configurable storage circuit 120. Signals A,
11 C, and D are also input signals to storage circuit 120.
12 Configurable storage circuit 120 includes programmable
13 switches 122, 123, 126, 127 and 128, exclusive OR gates
14 124, 129 and 130, AND gates 125, 131 and 132, and storage
15 element 121. Storage element 121 has a set, reset, data
16 and clock input leads denoted by S, R, D and Ck, respec-
17 tively, and output leads Q_{FF} and Q_{LA} .

18 Switches 123, 126, 127 and 128 are each configured
19 to select one of their input signals as an output signal.
20 The set, clock, and reset functions associated with the
21 set, clock, and reset input leads of storage element 121
22 are all active high but each may be rendered active low
23 relative to the output signal of switches 123, 127, and
24 129 respectively by applying a logical 1 to the leads
25 INVS, INVC, and INVR of exclusive or gates 124, 129, and
26 130 respectively. (If a logical 0 is applied to leads
27 INVS, INVC, and INVR, the polarity of the output signals
28 of the exclusive-or gates 124, 129, and 130 is the same
29 as that of the input signals. If a logical 1 is applied
30 to leads INVS, INVC, and INVR, the output signals of
31 exclusive-or gates 124, 129, and 130 are the inverse of
32 the input signals.)

33 The AND gates 125, 131, and 132 are enabled by
34 applying a logical 1 to the input leads ENS, ENC, and ENR
35 respectively (and disabled by applying a logical 0). If
36 a logical 0 is applied to one of the input leads ENS,
37 ENC, or ENR, the output of the AND gate is a logical 0
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1 and the associated function of memory circuit 121 is
 2 disabled regardless of the state of the corresponding
 3 exclusive OR gate. Q_{FF} provides a flip-flop output
 4 signal and Q_{LA} provides a latch output signal as explained
 5 later in conjunction with Fig. 9. Configurable switch
 6 122 selects one of the binary signals on leads Q_{FF} and
 7 Q_{LA} and the output signal Q of switch 122 is an input
 8 signal to the output select logic 140 and to the configu-
 9 rable combinational logic 100.

10 Fig. 9 shows one embodiment of memory circuit 121.
 11 Memory element 121 comprises two "D" latches LA1 and LA2
 12 connected in series thereby implementing a flip-flop.
 13 Latch LA1 includes N channel pass transistors P1 and P2
 14 and NOR gates G1 and G2. The gates of pass transistors
 15 P_1 and P_2 are controlled by the signals \overline{CK} and CK, respec-
 16 tively. Similarly, latch LA2 includes N channel pass
 17 transistors P3 and P4 and NOR gates G3 and G4. The gates
 18 of transistors P3 and P4 are controlled by the signals CK
 19 and \overline{CK} , respectively. The D input lead is the data input
 20 lead of latch LA1. The S input lead serves as the set
 21 input lead of latch LA1 and as the reset input lead of
 22 latch LA2. The R input lead serves as the reset input
 23 lead of latch LA1 and as the set input lead of latch LA2.

24 The output signal \overline{Q}_{LA} of NOR gate G1 is connected to
 25 the data input lead of latch LA2. The output lead Q_{LA} is
 26 connected to the output lead of NOR gate G2 of latch LA1
 27 and the output lead Q_{FF} is connected to the output lead
 28 of NOR gate G3 of latch LA2.

29 Configurable storage circuit 120 (Fig. 8) operates
 30 as a transparent latch with set and reset by configuring
 31 switch 122 to connect output lead Q to output lead Q_{LA} .
 32 The output signal on lead Q_{LA} follows the input signal
 33 while the clock signal CK is low. The output signal on
 34 Q_{LA} is held when the clock signal CK goes high, turning
 35 off pass transistor P_1 and turning on pass transistor P_2 .
 36 Thus, the data signal is transmitted to output lead Q_{LA} .
 37
 38

1 Storage circuit 120 may also be configured to operate
2 as a D flip-flop with set and reset. In this configura-
3 tion, switch 126 is configured to select the signal on
4 lead F_1 and gates 125, 131 and 132 are enabled by applying
5 a logical 1 to leads ENS, ENC, and ENR, respectively.
6 Finally, switch 122 is configured to select the output
7 signal on lead Q_{FF} of storage element 121. Storage
8 element 120 may also be configured as a D flip-flop
9 without set and reset by modifying the above configura-
10 tion by applying a logical zero to leads ENS and ENR.

11 Configurable storage circuit 120 may also be config-
12 ured to be an RS latch by enabling AND gates 125 and 132,
13 and disabling AND gate 131 so that a logical 0 input
14 signal is provided on the Ck input lead of storage element
15 121. The logical 0 on lead Ck turns off pass transistor
16 P3 and turns on pass transistor P4. Switch 122 is then
17 configured to select the output signal on Q_{FF} .

18 Finally, storage circuit 120 may also be configured
19 to be an edge detector. For example, to configure storage
20 element 120 as a rising edge detector, AND gate 125 is
21 disabled to provide a logical 0 on input lead S, AND gate
22 131 is enabled to pass a clock signal to input lead Ck,
23 and switch 126 is configured to select input lead 126a so
24 that a logical 1 is provided to input lead D. AND gate
25 132 is enabled. A logical 1 reset signal forces the
26 output signal on Q_{FF} to a logical 0. A low clock signal
27 turns off pass transistor P2 and P3 and turns on pass
28 transistor P1, permitting NOR gate G1 to invert the
29 logical 1 on lead D, thus providing a logical 0 on node
30 \bar{Q}_{LA} . When the clock signal rises, transistors P1 and P4
31 are turned off, transistors P2 and P3 are turned on, and
32 the logical 0 on node \bar{Q}_{LA} is inverted by NOR gate 23,
33 thus providing a logical 1 on output lead Q_{FF} which
34 signals that a rising edge has been detected. Q_{FF} is
35 then reset to 0 using the reset input and the edge detector
36 is then ready to detect the next rising edge. (Note that
37 when the clock signal falls, transistors P2 and P3 are
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1 turned off and transistor P4 is turned on, and the signal
2 on Q_{FF} remains a logical 0 and does not change state
3 until the next rising edge.)

4 Similarly, storage circuit 120 may be configured as
5 a falling edge detector by applying a logical one signal
6 to lead INVC of exclusive-or gate 129. Clearly, storage
7 circuit 120 may also serve as a stage of a shift register
8 or a stage of a counter.

9 The output select logic 140 includes configurable
10 switches 141 and 142 which are each configured to select
11 an output signal from among the output signals on leads
12 F1 and F2 from the combinational logic 100 and the output
13 signal of storage element 120.

14 The above embodiments are intended to be exemplary
15 and not limiting. It will be obvious in view of the
16 disclosures made above that various substitutions and
17 modifications may be made without departing from the
18 scope of the invention.

19 In the claims which follow, the phrase "means having
20 a configuration in which said means" performs a particular
21 function is used in place of the detailed wording "means
22 which are capable of being configured in response to a
23 selected set of values of a set of configuration signals
24 and which, when configured by said selected set of values,"
25 performs a particular function.

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CLAIMS:

1. A configurable storage circuit for such a configurable logic element, comprising: memory means for storing data, said memory means having at least a first and a second input lead; a first set of one or more input leads corresponding to said first input lead, each input lead of said first set for receiving a corresponding input signal; a second set of one or more input leads corresponding to said second input lead, each input lead of said second set for receiving a corresponding input signal; first means which, for each given lead in said first set, has a corresponding configuration in which said first means provides the input signal on said given lead to said first input lead; second means which, for each given lead in said second set, has a corresponding first configuration in which said second means provides the input signal on said given lead to said second lead; said memory means generating one or more output signals in response to said signals provided by said first means and said second means.

2. A configurable storage circuit as in claim 1, wherein said second means, for some given lead in said second set, has a corresponding second configuration for providing the complement of the signal on said some given lead to said second lead.

3. A configurable storage circuit as in claim 1, wherein said second means includes means for generating a first constant signal and has a configuration in which said second means provides said first constant signal to said second lead.

4. A configurable storage circuit as in claim 3,
wherein said second means includes means for selecting
between providing said first selected one of said input
signals of said configurable storage circuit to said
5 second input lead and providing the inverse of said first
selected one of said input signals to said second input
lead.

5. A configurable storage circuit substantially as
10 hereinbefore described with reference to the
accompanying drawings.

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